Power Aware Distributed Systems

DARPA PAC/C Review

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0900 – Introduction
  - Project Overview, Milestones Summary, Financial Status

0930 – Algorithms
  - Video Processing, Acoustic Beamforming

1000 – Middleware, Tools, and Techniques
  - Power Aware RTOS, Network Wide Power Management

1030 – Architectural Approaches
  - Research Platform Testbed, Reconfigurable Radio

1100 – Joint Spectrum Center / IIT Research Institute

1130 – Feedback, Action Items
**Power Aware Distributed Systems**

### Extending dynamic power range for distributed sensor networks.

**Impact**
- Power-aware algorithms, sensor node RTOS, and middleware will reduce sensor network aggregate energy requirements >1000X.
- This capability will extend sensor network power dynamic range to span from prolonged (months) quiescent operation to “get me the information now at any cost”.
- Power instrumentation of existing low-power sensor node provides baseline by which PAC/C tools and technology will be measured.

**Goals**
- **Algorithms.** Develop power-aware algorithms for cooperative signal processing that exploit sensor data locality, multi-resolution processing, sensor fusion, and accumulated intelligence.
- **Protocols.** Design a distributed sensor network control middleware for power-aware (P-A) task distribution and hardware/software resource utilization migration.
- **Compilers/OS.** Create sensor node RTOS to manage key resources – processor, radio, sensors.
- **Systems.** Identify hardware power control knobs and readable parameters and make them available to the sensor node power-aware RTOS.

**Milestones [FY/Q]**
- P-A RTOS scheduling on research platform [01/Q1].
- Instrumentation board for research platform [01/Q1].
- Compressed image transmission (Laplacian Pyramid) [01/Q1].
- SensorSim simulation tool with P-A extensions [01/Q4].
- Tool for power-aware RTOS kernel synthesis [02/Q4].
- Deployable platform with P-A control “knobs” [02/Q4].
- P-A network resource allocation DP field demo [03/Q2].
- RP w/ sensor-triggered activation & low power sleep [03/Q3].
- High-res multi-look image classification demo [03/Q4].

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Cooperative Signal Processing

Sensor Network Middleware

Sensor Node Hardware Control Knobs and Power Aware RTOS
Q: How can you extend the dynamic power range of sensor networks from quiescent months of monitoring to frenetic minutes of activity?

- **Power Aware Algorithms**
  - Multi-Resolution Distributed Algorithms

- **Middleware, Tools, and Techniques**
  - Power Aware Resource Scheduling in RTOS
  - Techniques for Network-Wide Power Management

- **Architectural Approaches**
  - Power Aware Research Platform Testbed
  - Deployable Power Aware Sensor Platform
1. Instrument state-of-the-art node to understand power consumption. Where can we expect significant latitude in power tradeoff? Which knobs have greatest dynamic range? What baseline will we use for comparison?

2. Identify hardware knobs that can be provided by modules (radio and processor systems) that can be altered dynamically, and externally readable parameters (power, BER, signal strength, battery, etc.) that can be provided to a power-aware runtime system.

3. Provide operating system extensions for power management, task scheduling, and task control on individual sensor nodes.

4. Create reconfigurable communication modules that adapt parameters such as error control, equalization, data rate, and noise figure in real time according to channel state.
5. Design a distributed sensor network control middleware for power-aware task distribution and hardware/software resource utilization migration.

6. Incorporate power trade-off analysis tools into the SensIT platform emulator for power aware application development and scenario simulation for sensor networks.

7. Develop power-aware algorithms for cooperative signal processing that exploit sensor data locality, multiresolution processing, sensor fusion, and accumulated intelligence.

8. Integrate advanced power aware processing and communications technology into the PADS research platform as it becomes available in the PAC/C community.
Algorithm Deliverables

- Algorithm demonstration code in C for compressed image transmission with incremental resolution based on Laplacian Pyramid [FY01/Q1].
  - Source code completed and will be added to the PADS project web page.

- Multi-resolution acoustic beamforming code/demonstration [FY01/Q1].
  - Beamforming code has been received from ARL/MIT. Description available on PADS web page and CDs are being redistributed to PACC members following ARL tracking requirements.

- Multi-resolution image target classifier code w/ neural nets [FY02/Q1].
  - On schedule. Algorithm will utilize incremental LP image transmission.

- Multi-resolution, hierarchical sensor cueing algorithm w/ acoustic and/or low-res imaging sensor processing simulator demonstration [FY02/Q4].

- Directed high-resolution multi-look image classification/validation demo [FY03/Q4].
Middleware Deliverables 1/3

- P-A scheduling in RTOS lab demonstration on RP [FY01/Q1].
  - Done. RP was substituted by Intel Assabett board.

- RTOS power management simulation tool evaluation [FY01/Q2].
  - Done. We have created a PARSEC-based simulation framework for evaluating various RTOS power management policies.

- P-A resource management lab demonstration on RP [FY01/Q3].
  - Mostly on target. Algorithms for power aware communication resource management done (modulation scaling, and power-aware wireless link packet scheduling) developed, and simulated. However, no RP with appropriately capable radio is available. We are investigating creating our own demonstration platform this summer.

- RTOS power management simulation tool demonstration [FY01/Q4].

- P-A scheduling in RTOS field demonstration on DP [FY02/Q1].
  - On target assuming timely availability of DP. May defer to Summer ’02 (Q3).

- P-A resource management field demonstration on DP [FY02/Q1].
  - On target assuming timely availability of DP. May defer to Summer ’02 (Q3).

- RTOS power management simulation tool release [FY02/Q1].

- Integration of SensIT P-A protocols into PAC/C [FY02/Q1].
Middleware Deliverables 2/3

√ ■ Basic hybrid simulator with gateway to RSC nodes [FY00/Q2].
  □ Done/demonstrated with RSC uC/OS nodes.

! ■ Data collection during SensIT field demonstration using software instrumented RSC node [FY00/Q2].
  □ Initial setback due to late start of PADS project. Missed opportunity in March 2001 because of stability/availability of RSC WINS nodes. Minimal data captured. Next opportunity is November 2001. Reassess benefit?

~ ■ Power models of RSC nodes, protocols, and network traffic [FY01/Q3].
  □ Power models of RSC nodes done. RSC has not release protocol details, and probably won't for proprietary reasons. So the protocols in simulator are our own, and don't reflect the RSC node protocols. Network traffic data not available yet. However, we have created a tool called SensorVis to let us define our own network traffic scenarios.

! ■ Benchmark scenarios from RSC nodes and SensIT field data [FY01/Q4].
  □ Behind due to setback in SensIT data collection. Consider other datasets?

■ Hybrid simulation/emulation framework release [FY02/Q1].
  □ On schedule.
- Tool for P-A RTOS kernel synthesis with static scheduling [FY02/Q4].
- Synthesis tool w/ dynamically scheduled RTOS kernel [FY03/Q2].
- P-A network resource allocation simulation demonstration [FY02/Q3].
- P-A network resource allocation on DP, field demonstration [FY03/Q2].
- Algorithms for P-A network migration of H/W and S/W functions, demonstration on network of RP nodes with attached FPGA [FY03/Q1].
- Field demonstration of network migration using beam forming and multiresolution sensor processing algorithms [FY03/Q2].
Architecture Deliverables

~ ■ Instrumentation board for RP with RSC modules [FY01/Q1].
   □ Instrumentation board for overall power consumption of RSC node completed on schedule. Used at SITEX01 experiment. Power isolation boards for detailed analysis now in fabrication. Delay due to availability of RSC nodes.

! ■ FPGA radio with basic communication modules [FY01/Q1].
   □ The FPGA radio prototype has been assembled using the Xilinx Virtex development board. This deliverable to be completed next quarter. We are completing a prototype FPGA modem that has basic modes to enable power saving dynamic range. We are slightly behind the original schedule due to a late start. However, we are ramping up our efforts. Our plan is to have the prototype demonstrated during the June review.

■ Fine grain instrumented processor module for RP [FY02/Q1].
   □ On schedule assuming reference selected. Several references available.

■ Land Warrior streaming multimedia support [FY02/Q1].
   □ On target. Evaluated power management of software-based multimedia functions of audio encoding/decoding, and MPED decoding.

■ FPGA radio w/ RF amp and b/w adaptive analog interface [FY02/Q4].
   □ We have investigated preliminary adaptive RF architecture based on COTS components (e.g. RFMD).
FPGA radio w/ RF amp and b/w adaptive analog interface [FY02/Q4].
- We have investigated preliminary adaptive RF architecture based on COTS components (e.g. RFMD).

FPGA radio prototypes with run-time reconfiguration [FY02/Q2].
- We have developed a preliminary scheme to support run-time reconfiguration using Virtex FPGAs. The reconfiguration will be controlled by the processor.

Deployable platform (DP) with P-A control "knobs"/monitors [FY02/Q4].
- We are working on schematics for DP. A review of the schematic will take place during the middle of June.

DP with advanced RSC processor board and technology from RP [FY02/Q4].
- The transferable technology is still being defined.

RP with sensor-triggered activation to enable ultra-low power sleep mode, and technology integrated from RP [RSC/ISI: FY03/Q3].
- No progress.
Revised Proposed Funding Profile:
- FY00 $432K -> (assumed June '00 start)
- FY01 $1270K
- FY02 $1282K
- Total $2984K -> (FY03 $837K option not funded)

Awarded Funding Profile:
- FY00 $621K -> (award Aug '00, subs Oct '00)
- FY01 $906K -> (Nov '00)
- FY02 $707K
- FY03 $750K
- Total $2984K
Financial Status

- **Obligated Budget:** $1,527,201
- **Cumulative Expenses:** $420,033
- **Recorded Commitments:**
  - $179,815
  - $250,000 UCLA FY01
  - $250,000 RSC FY01
  - $679,815
- **Balance against obligated funds:**
  - $927,353
  - $679,815
  - $247,538

**Notes:**
- Late start at subs has delayed their efforts by 3-5 months.
- UCLA and RSC not distributed FY01 increment. This skewed balance against obligated funds. This has been corrected.
- ISI has deferred assigning hardware team pending selection of target research platform. This is happening now.
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SITEX01 Experiment

(ISI, VT, UCLA, Rockwell)

- Wave Intensity Comparison – multiple projections are made from seismic signal energy at sensor node clusters.
- Nine Rockwell HYDRA nodes.
- Laptop with web cam.
- COTS 802.11 wireless Ethernet bridge to base camp (~1km).

At Base Camp
- Situation status display GUI (running on laptop).
- Live video feed at 5fps on wireless iPAQ PDA.